Abstracts

Process Technology and Modeling of a Low-Noise Silicon Bipolar Transistor with Sub-Micron Emitter Widths

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A low-noise silicon bipolar transistor with a 0.7 µm emitter width has been developed using a self-aligning process combined with ion implantation and local oxidation. Experimental noise figures of 1.45 dB at 1.5 GHz and 2.7 dB at 4 GHz are typical of transistor wafers made with this process. The best result obtained at 4 GHz was a noise figure of 2.3 dB with an associated gain of 9.5 dB. A T-equivalent circuit based on a regional analysis and empirical time constants is shown to accurately predict transistor S-parameters in the 1 to 8 GHz frequency range. Good agreement between predicted and experimental amplifier noise figure is obtained between 0.4 and 6 GHz.

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